REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1, and 3 through 14 remain in this case. Claims 1, 3, 5 through 8, 11, and 14 are amended. Claim 2 is canceled.

Claims 3, 4, and 6 were rejected under §102 as anticipated by the Abbaszadeh reference[1].

Regarding independent claim 3, the Examiner asserted that the Abbaszadeh reference meets all of the limitations of the claims, including the processing of prolog elements which the Examiner found at column 4, lines 49 through 67 of the reference.[2] Specifically, the Examiner asserted that this portion of the reference teaches the processing of "D" as a prolog.[3]

Claim 3 is amended for clarity, and to clarify the novelty and patentability of it and its dependent claims 4 and 5 over the prior art. Amended claim 3 now expressly recites that the processing method is directed to the processing of a block of data in a sequence of blocks of data, and that the prolog elements in each of the sequentially processing steps are from an adjacent block relative to that being processed. The specification clearly supports this amendment to claim 3,[4] and therefore no new matter is presented by this amendment.

The method of claim 3 provides important advantages in data processing, especially in connection with maximum *a posteriori* (MAP) decoding of communicated data. More specifically, the claimed method permits accurate decoding of a block of data without requiring knowledge of the initial conditions at the ends of the data block, because the processing of the prolog elements efficiently derives these initial conditions.[5]

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[1] U.S. Patent No. 6,563,877 B1, issued May 13, 2003 to Abbaszadeh, filed March 31, 1999.
[2] Office Action of April 13, 2004, page 2, §1.
[3] *Id.*
[4] *See* specification of S.N. 09/772,499, page 11, line 17 through page 12, line 9.
[5] *Id.*

Applicants respectfully submit that the Abbaszadeh reference falls short of the requirements of amended claim 3. Nowhere does the reference anywhere disclose the sequential processing of data elements of a block of data, after first processing prolog elements from an adjacent block, as required by both of the sequentially processing steps of amended claim 3.

The Abbaszadeh reference, as pointed out by the Examiner[6], operates upon windows of data that are "of cycle size D".[7] There is no mention in the text of whether any of the elements of a size D window are from an adjacent window, or block of data as recited in claim 3. As such, there is no explicit disclosure in the Abbaszadeh reference of the processing of prolog elements from an adjacent block prior to sequentially processing data elements of a given block as required by amended claim 3.

Not only does the Abbaszadeh reference fail to expressly disclose the processing of data elements from adjacent blocks as claimed, but it instead shows that its processing *does not* process elements from adjacent windows or blocks. As shown in Figure 2 of the Abbaszadeh reference, the windows of size "D" are non-overlapping. This indicates that each data element in a given window is processed once and only once according to the Abbaszadeh reference, even if the element is at the beginning or end of a given window of size D. However, according to amended claim 3, prolog elements belong to an adjacent block in the sequence of blocks of data. This means that these prolog elements are necessarily processed at least twice -both in the processing of its own block, and also prior to processing an adjacent block. This necessitates that the sliding windows according to amended claim 3 will be overlapping.[8] The teachings of the Abbaszadeh reference therefore fall short of the requirements of amended claim 3 in this case.

For these reasons, Applicants submit that amended claim 3 and its dependent claim 4 are novel over the Abbaszadeh reference.

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[6] Office Action, *supra*, page 2, §1.
[7] Abbaszadeh, *supra*, column 5, lines 49 through 52.
[8] *See* specification, *supra*, Figure 8, and page 14, lines 11 through 20.

Applicants further respectfully submit that amended claim 3 and its dependent claims are patentably distinct over the prior art of record in this case.

As mentioned above, the Abbaszadeh reference falls short of the requirements of amended claim 3, because it fails to disclose first processing of prolog elements from an adjacent block, in the processing of data elements in a given block of data. The other references of record in this case fail to add any teachings in this regard. Accordingly, the combined teachings of the prior art fall short of the requirements of amended claim 3 and its dependent claims.

Applicants further submit that there is no suggestion from the prior art to modify these teachings in such a manner as to reach the method of amended claims 3 through 5. The Abbaszadeh reference derives its initial conditions for its decoding by performing the backward recursion twice; the first backward recursion is initialized with "all equal likelihood states" and the results from this first backward recursion determines the initial conditions for the second backward recursion.[9] But there is no suggestion from the Abbaszadeh reference to use prolog data elements from an adjacent block or window to derive the initial conditions. The Viterbi et al. reference[10] and the Van Stralen et al. reference[11], which were applied against other claims in this case, add no suggestion in this regard, as these references disclose the initialization of their processing steps with arbitrary values.[12] Especially considering that the important advantages provided by the claimed method, including the accurate decoding of a block of data without requiring knowledge of the initial conditions at the ends of the data block, derive directly from the difference between the method of amended claim 3 and the prior art, Applicants respectfully submit that amended claim 3 and its dependent claims are patentably distinct over the prior art of record in this case.

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[9] Abbaszadeh, *supra*, column 3, line 57 through column 4, line 4.
[10] U.S. Patent No. 5,933,462, issued August 3, 1999 to Viterbi et al.
[11] U.S. Patent No. 6,304,996 B1, issued October 16, 2001 to Van Stralen et al.
[12] Viterbi et al., *supra*, column 9, lines 63 through 66; Van Stralen et al., *supra*, column 7, lines 59 through 63.

Claim 5 is amended to further clarify its patentability over the prior art. Amended claim 5 now requires that each of the processing steps comprises a sequence of operations, and that each of those processing steps is pipelined so that a plurality of the operations in the sequence operate in parallel on different blocks. The specification of this application clearly supports this amendment to claim 5,[13] and as such no new matter is presented by this amendment to claim 5.

Applicants respectfully submit that amended claim 5 is further patentably distinct over the prior art. Nowhere do the applied references anywhere disclose the pipelining of different blocks in parallel, as required by amended claim 5, much less in combination with the processing of prolog elements as required by amended claim 3, upon which claim 5 depends. Especially considering the important advantages of accurate and efficient decoding by generating the initial states from the prolog elements, in combination with the improved computational efficiency from pipelining of the block processing, Applicants respectfully submit that amended claim 5 is further patentably distinct over the prior art of record in this case.

Claim 6 is also amended to overcome the §102 rejection. Each of the steps a) and b) of claim 6 now recite that the sequential processing of a sliding window block is performed after first processing prolog elements from an adjacent sliding window block. As discussed above relative to amended claim 3, the specification clearly supports this amendment to claim 6,[14] and as such no new matter is presented. The method of claim 6 also provides the important advantages discussed above relative to amended claim 3, including the accurate MAP processing in an efficient manner by deriving the initial states from prolog elements.

Similarly as discussed above relative to claim 3, Applicants submit that amended claim 6 is patentably distinct over the Abbaszadeh reference. Nowhere does the Abbaszadeh reference anywhere disclose the processing of prolog elements from an adjacent sliding window block prior to processing the elements of a sliding window block. Indeed, the sliding windows of the

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[13] *See* specification, *supra*, at page 13, lines 7 through 16; Figure 6.
[14] *See* specification of S.N. 09/772,499, page 11, line 17 through page 12, line 9.

Abbaszadeh reference are shown as non-overlapping,[15] which necessitates the conclusion that no processing of elements from an adjacent block is performed. For this reason, Applicants submit that amended claim 6 is novel over the Abbaszadeh reference.

Applicants further submit that amended claim 6 is patentably distinct over the Abbaszadeh reference and the other prior art of record in this case. The other applied references similarly fail to disclose the processing of prolog elements from an adjacent sliding window block, as required by amended claim 6, and therefore the combined teachings of the prior art in this case fall short of the requirements of the claim.

Furthermore, there is no suggestion from the prior art to modify these teachings in such a manner as to reach amended claim 6. As discussed above relative to claim 3, there is no suggestion from the Abbaszadeh reference, considering that it teaches processing each sliding window twice, with the first processing beginning from an equal-likelihood initial condition, and the second processing using the results from the first processing as its initial states.[16] The other references disclose only the initialization with arbitrary values,[17] and therefore add no suggestion in this regard. Proper consideration of the advantages of the method of amended claim 6, which directly result from the difference between the claim and the prior art, further supports the patentability of this claim.

For these reasons, Applicants respectfully submit that amended claim 6 is also patentably distinct over the prior art of record in this case.

Claims 1, 2, 5, 7, 8 through 10, and 11 through 13 were rejected under §103 as unpatentable over the Abbaszadeh reference in view of the Viterbi et al. reference.

Regarding claim 1, the Examiner asserted that the Abbaszadeh reference teaches all of the elements of the claim except for the pipelining of the sliding window operations relative to

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[15] Abbaszadeh, *supra*, Figure 2.
[16] Abbaszadeh, *supra*, column 3, line 57 through column 4, line 4.
[17] Viterbi et al., *supra*, column 9, lines 63 through 66; Van Stralen et al., *supra*, column 7, lines 59 through 63.

one another.[18] The Examiner found that the Viterbi et al. reference teaches the parallel operations recited by the claim, and that it would have been obvious to the skilled artisan to incorporate this pipelining into the Abbaszadeh method to minimize delay.[19]

Claim 1 is amended to overcome the rejection. Amended claim 1 now requires that each sliding window operation comprises a sequence of operations to be performed on each partial block of data, and that each of these sliding window operations is pipelined so that a plurality of the operations in that sequence operate in parallel on different ones of the partial blocks of data. Claim 2 is canceled accordingly. The specification clearly supports this amendment to claim 1,[20] and therefore no new matter is presented by this amendment. The method of claim 1 provides important advantages in MAP decoding, by taking advantage of the latency in the processing operations resulting from their composition as a sequence of operations.[21]

Applicants respectfully submit that the combined teachings of the applied references fall short of the requirements of amended claim 1. As mentioned above, the Examiner admitted that the Abbaszadeh reference fails to disclose pipelining, but that the Viterbi et al. reference teaches the pipelining of sliding window operations with each other.[22] The specific words of the Viterbi et al. reference in this regard read "it may be necessary to pipeline the successive iterations".[23] But this location of the Viterbi et al. reference does not disclose that each of the sliding window operations comprises a sequence of operations, and that each of these operations is pipelined so that a plurality of the operations in the sequence operate in parallel on different partial blocks of data, as recited in amended claim 1. Indeed, the Examiner interpreted this location of the reference as disclosing that the first and second sliding window operations operate in parallel with one another, on different partial blocks of data.[24] And the remainder of the Viterbi et al. reference clearly teaches that, in a given block of time L, each of the forward and backward processors is operating on one and only one block of branch

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[18] Office Action, *supra*, pages 3 and 4, §1.
[19] *Id.*, *citing* Viterbi et al., *supra*, column 11, lines 47 through 54.
[20] *See* specification, *supra*, at page 13, lines 7 through 16; Figure 6.
[21] Specification, *supra*, page 12, line 22 through page 13, line 16.
[22] Office Action, *supra*, page 4, *citing* Viterbi et al, *supra*, at column 11, lines 47 through 54.
[23] Viterbi et al, *supra*, at column 11, lines 49 and 50.

symbols.[25] Accordingly, Applicants respectfully submit that the Abbaszadeh and Viterbi et al. references fail to disclose the pipelining of each of the sliding window operations in the manner recited in amended claim 1.

The other references of record also lack teachings in this regard.

Accordingly, Applicants respectfully submit that the combined teachings of the prior art of record in this case fall short of the requirements of amended claim 1.

Applicants further respectfully submit that there is no suggestion from the prior art or otherwise to modify these teachings in such a manner as to reach amended claim 1. As mentioned above, the Abbaszadeh reference lacks teachings in this regard, and the Viterbi et al. reference clearly discloses that each iteration or operation executes on one and only one block of symbols within a given time period.[26] To the extent that the Viterbi et al. reference suggests pipelining its decoding operation, as discussed above, this pipelining at best suggests the parallel operation of the forward and backward iterations among themselves, with no suggestion of pipelining so that a plurality of operations within each sliding window operation operates in parallel on different partial blocks of data as claimed. There is simply no suggestion to provide such pipelining in this decoding method, especially considering the advantages provided by this advanced pipelining, which further support the patentability of this claim.

For these reasons, Applicants respectfully submit that amended claim 1 is patentably distinct over the prior art of record in this case.

Claim 8 is also amended to overcome the §103 rejection. Amended claim 8 recites that its method is for parallel MAP processing on a plurality of sliding window blocks of data, and specifically recites that its step of combining probability metrics is performed on a first sliding window block of data, its maximum-finding operation is performed on a first previous sliding window block of data, and that these steps are at least partly performed in a parallelized

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[24] Office Action, *supra*, page 4.
[25] Viterbi et al., *supra*, column 10, line 48 through column 11, line 14.
[26] *Id.*

pipeline relationship with one another. The specification clearly supports this amendment to claim 8,[27] and as such no new matter is presented.

The method of amended claim 8 provides important advantages in the parallel MAP processing of communicated data, particularly in taking advantage of multiple stage latency to efficiently generate decoded output.[28]

Claim 11 is amended for consistency with amended claim 8 upon which it now depends, for the sake of clarity.

Applicants respectfully submit that amended claim 8 is patentably distinct over the prior art applied by the Examiner, because the combined teachings of the applied references fall short of the requirements of the claim. Applicants agree with the Examiner that the Abbaszadeh reference fails to disclose pipelining.[29] But Applicants submit that pipelining disclosed by the Viterbi et al. reference refers to the pipelining of sliding window operations with each other, and not the pipelining of operations within a sliding window operation, much less in the manner recited by amended claim 8. Indeed, the Examiner interpreted this location of the reference as disclosing that the first and second sliding window operations operate in parallel with one another on different partial blocks of data.[30] Instead, as mentioned above, the Viterbi et al. reference clearly teaches that, within a given block of time L, each of the forward and backward processors is operating on one and only one block of branch symbols.[31] Accordingly, Applicants respectfully submit that the Abbaszadeh and Viterbi et al. references fail to disclose the parallel pipeline relationship between the specific operations of combining probability metrics on a first sliding window block of data, and performing a maximum-finding operation on a first previous sliding window block of data, as recited in amended claim 8. And the other references of record also lack teachings in this regard.

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[27] Specification, *supra*, page 13, lines 7 through 16; Figure 6.
[28] Specification, *supra*, page 12, line 22 through page 14, line 10.
[29] Office Action, *supra*, page 4, *citing* Viterbi et al, *supra*, at column 11, lines 47 through 54.
[30] Office Action, *supra*, page 4.
[31] Viterbi et al., *supra*, column 10, line 48 through column 11, line 14.

Accordingly, Applicants respectfully submit that the combined teachings of the prior art of record in this case fall short of the requirements of amended claim 8.

Applicants further respectfully submit that there is no suggestion from the prior art or otherwise to modify these teachings in such a manner as to reach amended claim 8. As mentioned above, to the extent that the references, specifically the Viterbi et al. reference, teach the detailed operations within MAP processing as recited in amended claim 8, there is no suggestion that these are to be performed on different sliding window blocks of data in a parallel pipelined manner, as required by amended claim 8. Especially considering the advantages provided by this advanced pipelining, which further support the patentability of this claim, Applicants submit that amended claim 8 and its dependent claims are patentably distinct over the prior art of record in this case.

For these reasons, Applicants respectfully submit that amended claim 8 and its dependent claims 9 through 13 are patentably distinct over the prior art of record in this case.

Claim 14 was rejected under §103 as unpatentable over the Abbaszadeh and Viterbi et al. references, further in view of the Van Stralen et al. reference.

Claim 14 is amended to clarify its patentability over these references. Amended claim 14 now recites that each of the alpha and beta generation processes is divided into multiple pipelining stages, and that these stages operate on multiple sliding window blocks using alpha and beta prologs, respectively. The amendment to claim 14 is fully supported by the specification,[32] and therefore no new matter is presented by this amendment.

Applicants respectfully submit that amended claim 14 is patentably distinct over the applied references.

Similarly as discussed above relative to claims 1 and 8, the Abbaszadeh and Viterbi et al. references fail to disclose the multiple pipelining of stages within a process (*i.e.*, an alpha

[32] *See* specification, *supra*, at page 13, lines 7 through 16; Figure 6.

generation process and a beta generation process); at most, the Viterbi et al. reference teaches the parallel operation of iterations, or recursive processes, with one another.

Regarding claim 14, however, the Examiner asserted that the Van Stralen et al. reference teaches the operation of alpha and beta operations in parallel with one another.[33] But these teachings do not disclose that the alpha and beta generation processes themselves are divided into multiple pipelining stages to operate on multiple sliding window blocks, as required by amended claim 14. And, as discussed above relative to claims 3 and 6, Applicants respectfully submit that none of the references disclose MAP processes that operate on prologs. For these reasons, Applicants respectfully submit that the combined teachings of the applied references fall short of the requirements of amended claim 14.

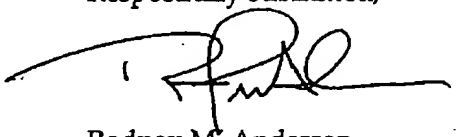
Applicants further respectfully submit that there is no suggestion from the prior art to modify the teachings of these references in such a manner as to reach amended claim 14. As mentioned above, there is no indication from these references that the specific operations involved within the overall iterative processes of MAP processing should be, or can be, pipelined, nor any suggestion that this pipelining can be implemented so that a given process operates on multiple sliding window blocks.

Accordingly, Applicants respectfully submit that amended claim 14 is also patentably distinct over the prior art of record in this case.

[33] Office Action, *supra*, page 6, *citing* Van Stralen et al., *supra*, at column 1, line 45 through column 2, line 5.

For the above reasons, Applicants respectfully submit that all claims now in this case are in condition for allowance. Reconsideration of this application is therefore respectfully requested.

Respectfully submitted,



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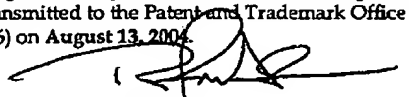

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